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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/601,959	06/23/2003	Chang-Hyeon Lee	050324-1321	8906
24504	7590	01/02/2004	EXAMINER	
THOMAS, KAYDEN, HORSTEMEYER & RISLEY, LLP 100 GALLERIA PARKWAY, NW STE 1750 ATLANTA, GA 30339-5948			CUNNINGHAM, TERRY D	
			ART UNIT	PAPER NUMBER
			2816	

DATE MAILED: 01/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

AD

Office Action Summary	Application No. 10/601,959	Applicant(s) LEE ET AL.	
	Examiner Terry D. Cunningham	Art Unit 2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-38 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-38 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 23 June 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) ☐ All b) ☐ Some * c) ☐ None of:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 13) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.
 a) ☐ The translation of the foreign language provisional application has been received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). ____. |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) <u>06/23/2003</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, both the “first and second voltage divider circuits”, as recited in claim 6, must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

Claims 26 and 27 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. It is not understood how a “charge pump” can further comprising “a phase lock loop”.

Claim Rejections - 35 USC § 112

Claims 1-29 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, lines 5-7, the phrase “where the drain terminals of the first input transistor and the first complementary transistor and the drain terminals connected with a source terminal of the first discharging transistor” is not understood. It appears that “and the drain terminals” in line 6 should be changed to --are--. Lines 12-14 are indefinite for similar reasons as lines 5-7. Thus,

similarly, it appears that “and the drain terminals” in line 13 should be changed to --are--. In lines 8 and 15, there is no support for the “first reference signal” and the “second reference signal”. As seen in Fig. 3, the “first complementary transistor” and the “second complementary transistor” both receive Vb. Thus, it is deemed misdescriptive to recite Vb as two separate signals. In lines 16-18, there is no support found for the “first and second output nodes” or the “differential pair output signal”. As seen in Figs. 3 and 5, the circuit only has one output providing one signal Vcp.

Claims 2-27 are rejected as including the indefiniteness discussed above with claim 1.

In claim 6, there is no support for both the “first and second voltage divider circuits”. As seen, Fig. 3 only discloses one such “voltage divider circuit”.

In claim 12, there is no support for the “first biasing signal” and the “second biasing signal”. As seen in Fig. 3, the “first discharging transistor” and the “second discharging transistor” both receive BIAS. Thus, it is deemed misdescriptive to recite BIAS as two separate signals.

In claim 23, there is no antecedent for “the UP and DW signals”.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United

States

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 10-24, 28 and 29 are rejected under 35 U.S.C. 102(b) as being anticipated by Lee (USPN 5,889,437). Lee discloses, in Fig. 7, a circuit comprising: “a first input stage” having “a first input transistor (M41)”, “a first complementary transistor (M42)”, “a first discharging transistor (M45)” and “a charging transistor (M47)”; “a first control signal (UP)”; “a first reference signal (\overline{UP})”; “a second input stage” having “a second input transistor (M43)”, “a second complementary transistor (M44)”, “a second discharging transistor (M46)” and “a charging transistor (M50)”; “a second control signal (DN)”; “a second reference signal (\overline{DN})”; and “a loop filter (R1, C1, C2)”, all connected and operating similarly as recited by Applicant.

With respect to claims 28 and 29, clearly the above circuit to Lee will provide the recited method.

Claims 30, 32 and 38 are rejected under 35 U.S.C. 102(b) as being anticipated by Kawasaki (USPN 5,955,904). Kawasaki discloses, in Fig. 4, a circuit comprising: “a first transistor pair, comprising a first switching transistor (50) and a first complementary transistor (51)”, all connected and operating similarly as recited by Applicant.

Claims 1-38 are rejected under 35 U.S.C. 102(e) as being anticipated by Qu (USPN 6,292,061, cited by Applicant). Qu discloses, in Fig. 3, a circuit comprising: “a first input stage” having “a first input transistor (left-most transistor, receiving F2 at the gate)”, “a first complementary transistor (second from left-most transistor, receiving XO at the gate)”, “a first

discharging transistor (left-most transistor receiving vn1 or vn2)” and “a charging transistor (left-most diode-connected transistor on top)”;

“a first control signal (dn, received via transistor having its drain connected to F2)”;

“a first reference signal (XO)”;

“a second input stage” having “a second input transistor (third from left-most transistor, receiving F1 at the gate)”;

“a second complementary transistor (fourth from left-most transistor, receiving XO at the gate)”;

“a second discharging transistor (transistor receiving XD at the drain)” and “a charging transistor (transistors coupled between XA and Vdd)”;

“a second control signal (up, received via transistor having its drain connected to F1)”;

“a second reference signal (\overline{DN})”;

“a voltage divider (series of resistors and transistor between vss and vdd)”;

and “a loop filter (RFILTER1, REFILTER2, C1F1, C2F1, C1F2 AND C3F2)”.

With respect to claims 26 and 27, reference is further made to Fig. 2 of Qu which discloses a phase lock loop circuit comprising a phase and frequency detector (105); and “a voltage-to-current converter (120)”.

With respect to claims 28 and 29, clearly the above circuit to Qu will provide the recited method.

With respect to claims 30-38, the above circuit to Qu discloses, in Fig. 4, a circuit comprising: “a first transistor pair” having “a first switching transistor (left-most transistor, receiving F2 at the gate)”;

“a first complementary transistor (second from left-most transistor, receiving XO at the gate)”;

“a first current source (left-most diode-connected transistor on top)” and “a first current sink (left-most transistor receiving vn1 or vn2)”;

“a first control signal (dn, received via transistor having its drain connected to F2)”;

“a constant bias voltage (XO)”;

“a second transistor pair” having “a second switching transistor (third from left-most transistor, receiving F1 at the gate)”;

“a second complementary transistor (fourth from left-most transistor,

Art Unit: 2816

receiving XO at the gate)”; and “a first cascode transistor pair (first cascode pair from left connected to vdd)”, all connected and operating similarly as recited by Applicant.


Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Terry Cunningham whose telephone number is 703-308-4872. The examiner can normally be reached on Monday-Thursday from 7:30 to 6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner’s supervisor, Timothy P. Callahan can be reached on 703-308-4876. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is 703-308-0956.

TC
December 24, 2003


Terry D. Cunningham
Primary Examiner
Art Unit 2816